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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/049,520	05/06/2002	Tomohiro Kashima	SON-2123/SOH	4074

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EXAMINER	
PRIZIO JR, PETER	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/049,520	KASHIMA ET AL.	
	Examiner	Art Unit	
	Peter Prizio	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed on 06 July 2004.

Claim Status

1. Claims 1 – 15 are pending with claims 1, 3, and 5 having been amended and claims 7 – 15 have been newly added.

2. Claims 1 – 15 are rejected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1 – 15** are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication 2003/0201964 to Murade.

4. Regarding claims 1, 3, and 5 Murade teaches a display device (Figs 1 – 4) comprising:

- A pixel part (9a) arranged in a matrix and having a signal line (6a) arranged for each pixel string (paragraph 67)

- A clock generating means (101) for generating a first clock signal (CLX) and a first inverse clock signal (CLX') having inverse phases to each other (see fig. 4, CLX and CLX' are shown to have inverse phases to each other) and a second clock signal (ENB2) and a second inverse clock signal (ENB1) having the same period and a smaller duty ratio than the first clock signal (again in fig. 4, the clock signals CLX and CLX' are shown to have the same period as ENB1 and ENB2 while the signals ENB1 and ENB2 are shown to have a smaller duty cycle)
- A shift register (400) for performing a shift operation in synchronization with said first clock signal and said first inverse clock signal (outputting a shift pulse in sequence from the shift stages (ST1 to STn)
- A first switch group (402) for sampling said second inverse clock signal or said second clock signal (ENB1 or ENB2 input to NAND 403, paragraph 79) in response to a shift pulse output in sequence from said shift register (ST1 to STn input to NAND 403)
- A second switch group (301) for sampling an input video signal (VID1 to VID12) in sequence in response to said second inverse clock signal or said second clock signal sampled (X1 to Xn) by the switches of the first switch group (402, paragraph 79) and supplying the sampled input video signal to the signal lines of the pixel part (S1 to Sn)
- Said second switch group (301) samples the input video signal in response to said second inverse clock signal (CLX') and supplies the sampled input video

signal to said signal lines arranged in the odd columns (paragraph 79 where the signal ENB2 corresponds to the odd numbered NAND gates 402 and therefore will correspond to the odd columns) and samples the input video signal in response to said second clock signal and supplies the sampled input video signal to said signal lines arranged in the even columns (paragraph 79 where the signal ENB2 corresponds to the even numbered NAND gates 402 and therefore will correspond to the even columns).

5. Regarding claims 2, 4, and 6 Murade, as applied to claims 1, 3 and 5 above further teaches a display device wherein a display element of each pixel of said pixel part is a liquid-crystal cell (paragraph 67).

6. Regarding claims 7, 10, and 13, Murade, as applied to claims 1, 3, and 5 above further teaches:

- a pulse repetition period is said same period, (again see fig. 4 the period of CLX)
- the duty ratio of the first clock signal (CLX) is the ratio of a first clock signal pulse width for the first clock signal to the pulse repetition period, said first clock signal pulse having a repetition rate of once per said pulse repetition period (by definition, the duty ratio of a pulse is the ratio of the on time versus the off time of a pulse therefore the duty ratio of CLX would be the pulse width over the total period i.e. the pulse repetition period)
- the duty ratio of the first inverse clock signal (CLX') is the ratio of a first inverse clock signal pulse width for the first inverse clock signal to the pulse

repetition period, said first inverse clock signal pulse having a repetition rate of once per said pulse repetition period (since the period is the same as CLX, the duty ratio can be calculated in a similar manner),

- the duty ratio of the second clock signal (ENB2) is the ratio of a second clock signal pulse width for the second clock signal to the pulse repetition period, said second clock signal pulse having a repetition rate of once per said pulse repetition period (by definition, the duty ratio of a pulse is the ratio of the on time versus the off time of a pulse therefore the duty ratio of ENB2 would be the pulse width over the total period i.e. the pulse repetition period),
- and the duty ratio of the second inverse clock signal (ENB1) is the ratio of a second inverse clock signal pulse width for the second inverse clock signal to the pulse repetition period, said second inverse clock signal pulse having a repetition rate of once per said pulse repetition period (since the period is the same as ENB1, the duty ratio can be calculated in a similar manner).

3. Regarding claims 8, 11, and 14, Murade, as applied to claims 1, 3, and 5 above further teaches the first clock signal (CLX) and the first inverse clock signal (CLX') have the same duty ratio (see the waveforms as illustrated in fig. 4 for CLX and CLX' and paragraph 78).

4. Regarding claims 9, 12, and 15, Murade, as applied to claims 8, 11, and 14 above further teaches the duty ratio the first clock signal (CLX) and the first inverse clock signal (CLX') is 50% (see CLX and CLX' from fig. 4, the waveforms are on for half the time and therefore have a 50% duty ratio)

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following publications have been included to further show the art that contains inverted first and second clock signals within an LCD driving circuit:

US Patent Application Publication 2002/0063676

US Patent Application Publication 2001/0022572

Response to Arguments

7. Applicant's arguments filed 06 July 2004 have been fully considered but they are not persuasive.

8. Applicant argues:

> While Murade arguably teaches the second clock signal ENB1 and a second inverse clock signal ENB2 having the same period as the first clock signal CLX and the first inverse clock signal CLX', Murade fails to disclose, teach or suggest the second clock signal ENBI and the second inverse clock signal having a smaller duty ratio than the first clock signal CLX and the first inverse clock signal CLX'

However, the argument is directed to the newly added limitation of a first inverse clock signal and the added limitation of a second inverse clock signal and therefore a new grounds of rejection as necessitated by the amendment has been provided to reject the amended claims. In reply, Murade teaches:

> A pixel part (9a) arranged in a matrix and having a signal line (6a) arranged for each pixel string (paragraph 67), a clock generating means (101) for generating a first clock signal (CLX) and a first inverse clock signal (CLX') having inverse phases to each other (see fig. 4, CLX and CLX' are shown to have inverse phases to each other) and a second clock signal (ENB2) and a second inverse clock signal (ENB1) having the same period and a smaller duty ratio than the first clock signal (again in fig. 4, the clock signals CLX and CLX' are shown to have the same period as ENB1 and ENB2 while the signals ENB1 and ENB2 are shown to have a smaller duty cycle), a shift register (400) for performing a shift operation in synchronization with said first clock signal and said first inverse clock signal (outputting a shift pulse in sequence from the shift stages (ST1 to STn), a first switch group (402) for sampling said second inverse clock signal or said second clock signal (ENB1 or ENB2 input to NAND 403, paragraph 79) in response to a shift pulse output in sequence from said shift register (ST1 to STn input to NAND 403), a second switch group (301) for sampling an input video signal (VID1 to VID12) in sequence in response to said second inverse clock signal or said second clock signal sampled (X1 to Xn) by the switches of the first switch group (402, paragraph 79) and supplying the sampled input video signal to the signal lines of the pixel part (S1 to Sn), said second switch group (301) samples the input video signal in response to said second inverse clock signal (CLX') and supplies the sampled input video signal to said signal lines arranged in the odd columns (paragraph 79 where the signal ENB2 corresponds to the odd numbered NAND gates 402 and therefore will correspond to the odd columns) and samples the input video signal in response to said second clock signal and supplies the sampled input video signal to said signal lines arranged in the even columns (paragraph 79 where the signal ENB2 corresponds to the even numbered NAND gates 402 and therefore will correspond to the even columns). (See above rejection).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter Prizio whose telephone number is (703) 305-5712. The examiner can normally be reached on Monday-Friday (7:30-5:00), alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Peter Prizio
Examiner
Art Unit 2674

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Henry N. Tran

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PRIMARY EXAMINER